# Dual LDO Monolithic IC MM3549 Series

#### Outline

MM3549 are dual LDO by small package. The IC are used for a smart phone's and mobile phone's RF or CMOS sensor power supply by high PSRR and load response. 300mA \*2ch, PLP-8 (1216size)

#### Features

- 1. Maximum input voltage
- 2. Maximum operating voltage
- 3. No load input current
- 4. Quiescent current (OFF)
- 5. Output voltage range
- 6. Output voltage accuracy
- 7. Dropout voltage
- 8. Line regulation
- 9. Load regulation
- 10. Vout temperature coefficient
- 11. Output NMOS ON resistance
- 12. Output Capacitor

7V 6V 40μA typ. (1ch) 0.1μA typ. (Vce=0V) 1.2 to 5.0V (0.1V step)  $\pm 1.0\%/\pm 20$ mV (Vo $\leq 2$ V) 0.22V typ. (Io=300mA, Vo=3V) 0.1%/V max. 40mV max. (Io=1 to 300mA)  $\pm 100$ ppm/°C typ. 10Ω typ. 1.0μF

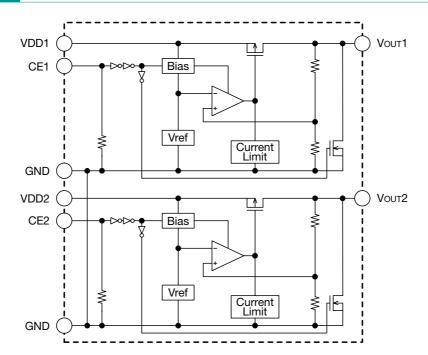
#### Package

PLP-8E

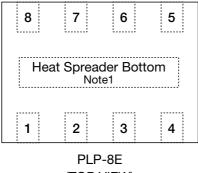
## Applications

- 1. Smart phone
- 2. Mobile phone
- 3. DSC

# **Block Diagram**



# Pin Assignment



(TOP VIEW)

1	GND
2	Vout1
3	Vout2
4	GND
5	CE2
6	VDD2
7	VDD1
8	CE1

Note1 : Heat Spreader Bottom with GND.

## **Pin Description**

Pin No.	Pin name	Functions
1, 4	GND	GND pin Please connect the terminal GND mutually when you mount the substrate.
2	Vout1	Output pin
3	Vout2	Output pin
4, 6	CE2, CE1	ON/OFF-Control pin         CE       OUTPUT         L       OFF         H       ON         Connect CE pin with VDD pin, when it is not used.
6, 7	VDD2, VDD1	Voltage-Supply pin

## Absolute Maximum Ratings (Except where noted otherwise Ta=25°C)

Item	Symbol	Ratings	Units
Storage Temperature	Tstg	-55~+150	°C
Junction Temperature	T <sub>jMAX</sub>	150	°C
Supply Voltage 1, 2	VDD1, VDD2	-0.3~+7.0	V
CE1, 2 input Voltage	VCE	-0.3~+7.0	V
Output Voltage 1, 2	Vout1, 2	-0.3~+7.0	V
Output Current 1	Iomax1	400	mA
Output Current 2	Iomax2	400	mA
Power Dissipation (Note1)	Pd	1250	mW

Note1 : JEDEC51-7 standard 114.3mm × 76.2mm t=1.6mm

# Recommended Operating Conditions (Except where noted otherwise Ta=25°C)

Item	Symbol	Ratings	Units
<b>Operating Ambient Temperature</b>	Topr	-40~+85	°C
Operating Junction Temperature (Note2)	Tjop	125	°C
Operating Voltage	Vop	1.6~6.0	V
Output Current 1, 2	Іор	0~150	mA

Note2 : In consideration of product life, the use in less than 80% of Tjop(max.) is recommended.

# Electrical Characteristics 1 (Except where noted otherwise VDD=VOUT(TYP.)+1V, VCE=VDD, Ta=25°C)

Item	Symbol	Measurement conditions	Min.	Тур.	Max.	Units
Input Current (OFF)	Iddoff	V <sub>CE</sub> =0V It is a value for each 1ch.		0.1	1.0	μΑ
No-Load Input Current	Idd	Iout=0mA It is a value for each 1ch.		40	80	μΑ
Output Voltogo 1	Vout1	Iouт=1mA, Vouт≧2.0V	×0.99		×1.01	v
Output Voltage 1	VOULI	Iouт=1mA, Vouт≦2.0V	-0.020		+0.020	
Output Voltage 0 (Nate 2)	Vout2	Iouт=1mA, Vouт≧2.0V -40≦Topr≦85°C	×0.97		×1.03	
Output Voltage 2 (Note3)	VOUTZ	Iouт=1mA, Vouт≦2.0V −40≦Topr≦85°C	-0.060		+0.060	V
		Vour(typ.)+0.5V≦VDD≦6.0V Iour=1mA, Vour>1.5V		0.02	0.10	%/V
Line Regulation VL		2.0V≦Vdd≦6.0V Iout=1mA, Vout≦1.5V		0.02	0.10	%/ V
Load Regulation	VLOAD	1mA≤Iouт≤300mA		10	40	mV
Dropout Voltage	Vio	Please refer to another page				V
Output Short-Circuit Current (Note3)	Ishort	Vout=0V		40		mV
Vout Temperature Coefficient (Note3)	⊿Vout/⊿Top	Iouт=1mA −40≦Top≦85°C		±100		ppm/°C
Ripple Rejection (Note3)	RR	f=1kHz, Vripple=0.5V, Iour=30mA		65		dB
CE High Threshold Voltage	VCEH		1.0		6.0	V
CE Low Threshold Voltage	VCEL				0.4	mA
CE Pin Current (Note3)	ICE			0.3		μA
Output Noise Voltage (Note3)	Vn	Bw=10Hz to 100kHz Iout=10mA		100		μVrms
Output NMOS ON Resistance (Note3)	Rdon			10		Ω

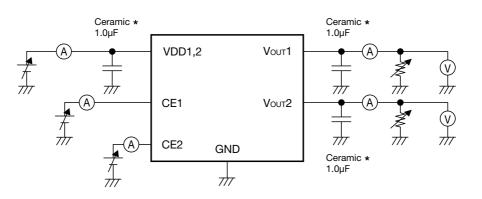
Note3 : The parameter is guaranteed by design.

# Electrical Characteristics 2 (Except where noted otherwise VDD=VOUT(TYP.)+1V, VCE=VDD, Ta=25°C)

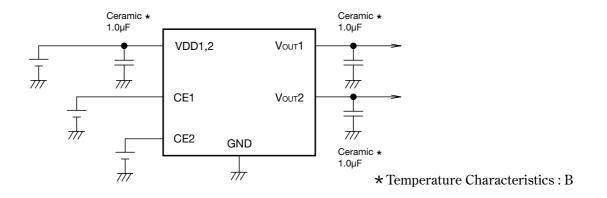
				lte	em			
Output Voltage		ut Volta	ge			out Volta	ge	
<b>V</b> out <b>(V)</b>		/оит <b>(V)</b>	_		1	Vio (V)	_	
4.00	Measurement Conditions	Min.	Typ.	Max.	Measurement Conditions	Min.	Тур.	Max.
1.20	-	1.180	1.200	1.220	-		0.39	0.50
1.30		1.280	1.300	1.320	-			
1.40		1.380	1.400	1.420			0.05	
1.50		1.480	1.500	1.520	Iout=300mA, 1.2V≦Vout≦2.0V		0.35	0.44
1.60		1.580	1.600	1.620	(Note4)			
1.70		1.680	1.700	1.720				
1.80		1.780	1.800	1.820			0.30	0.39
1.90		1.880	1.900	1.920	_			
2.00		1.980	2.000	2.020				
2.10		2.079	2.100	2.121	_			
2.20		2.178	2.200	2.222	_		0.26	0.34
2.30		2.277	2.300	2.323 2.424	_			
2.40		2.376 2.475	2.400		-			
2.50			2.500 2.600	2.525	_			
2.00		2.574 2.673	2.600	2.626 2.727	-			
2.70		2.073	2.700	2.121	-		0.25	0.30
2.80		2.112	2.800	2.828	-			
2.85		2.822	2.830	2.879	-			
3.00		2.970	3.000	3.030				
3.10	IOUT=1mA	3.069	3.100	3.131	-			
3.20		3.168	3.200	3.232	-			
3.30		3.267	3.300	3.333	-			
3.40		3.366	3.400	3.434	Iout=300mA,			
3.50		3.465	3.500	3.535	2.0V <vout≦5.0v< td=""><td></td><td></td><td></td></vout≦5.0v<>			
3.60		3.564	3.600	3.636	VDD=VOUT(TYP.)-0.2V			
3.70		3.663	3.700	3.737				
3.80		3.762	3.800	3.838	-			
3.90		3.861	3.900	3.939	-			
4.00		3.960	4.000	4.040	_		0.22	0.29
4.10		4.059	4.100	4.141	_		0.22	0.20
4.20		4.158	4.200	4.242	-			
4.30		4.257	4.300	4.343				
4.40		4.356	4.400	4.444	-			
4.50		4.455	4.500	4.545				
4.60		4.554	4.600	4.646				
4.70		4.653	4.700	4.747				
4.80		4.752	4.800	4.848	-			
4.90		4.851	4.900	4.949	-			
5.00		4.950	5.000	5.050	-			

Note4 : It applies dropout voltage MAX level to an input terminal, include a load regulation and confirms that the output voltageis less than ±60mV at load 300mA (Vout≦2.0V).

### **Measuring Circuit**



# **Application Circuit**



- (Reference example of external parts)
- $\cdot \ Output \ capacitor \qquad \qquad Ceramic \ capacitor \ 1.0 \mu F$
- · Input capacitor Ceramic capacitor 1.0μF
- In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

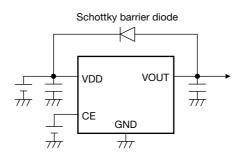
· Note

1. There is a possibility with deterioration and destruction of IC when using it exceeding the absolute maximum rating.

The absolute maximum rating, Never exceed it.

The functional operation is not assured.

- There is a possibility that it becomes impossible to maintain this performance and reliability IC original when using it exceeding recommended operation voltage.
   Please use it in recommended operation voltage.
- 3. Due to restrictions on the package power dissipation, the output current value may not be satisfied. Attention should be paid to the power dissipation of the package when the output current is large or the voltage between Input and Output is high.
- 4. The output capacitor is required between output and GND to prevent oscillation.
- The ESR of capacitor must be defined in ESR stability area.
   It is possible to use a ceramic capacitor without ESR resistance for output.
   The ceramic capacitor must be used more than 1.0µF and B temperature characteristics.
- 6. The wire of VDD and GND is required to print full ground plane for noise and stability.
- 7. The input capacitor must be connected a distance of less than 1cm from input pin.
- 8. In case the output voltage is above the input voltage, the overcurrent flow by internal parasitic diode from output to input. In such application, the external bypass diode must be connected between output and input pin.



- 9. It is able to an unstable operation when you use the capacitor with intense capacitance change The capacitor has the dependency at the power-supply voltage and the temperature.
- The capacity value changes by the environment used. Please evaluate IC in the set.
- 10. The overcurrent protection circuit of foldback current limit type is built into this IC.
- 11. This IC have not the thermal shutdown protection.
- 12. This IC will limit the output current with the overcurrent protection circuit when the overcurrent and the output do short-circuit.

However, IC generates heat because of the substrate and use conditions and there is a possibility of destroying it exceeding a permissible loss.

The characteristic changes depending on the substrate condition.

- Please evaluate IC in the set.
- 13. This IC has the pull-down function of the CE terminal.

The pull-down function uses the internal constant current source.

- 14. The short circuit electric current has dependence of the input voltage. Short circuit electric currents more than 100mA may flow (VDD≤2V).
- 15. Transient response characteristics may turn worse, when dropout voltage is less than 0.5V. When a dropout voltage does not have a margin, please evaluate it enough.
- 16. It may become unstable when output current is less than 10mA (Vout(typ.)<1.7V).
- 17. When the terminal VDD (CE) is OFF→ON, the overshoot might be generated. The size of the overshoot depends on "output capacity", "output load", a "voltage rank", and "VDD standup speed." and evaluate it enough with a real machine, please.

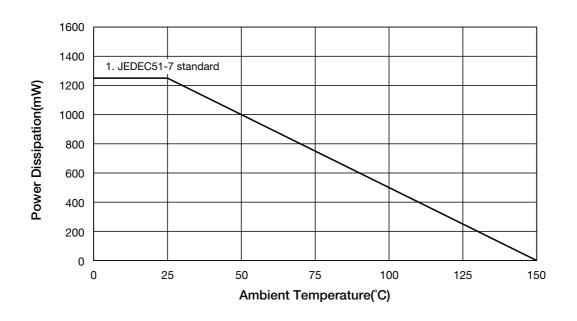
<sup>Any products mentioned in this catalog are subject to any modification in their appearance and others for improvements without prior notification.
The details listed here are not a guarantee of the individual products at the time of ordering. When using the products, you will be asked to check their specifications.</sup> 

### About Power Dissipation

The Power dissipation change if board to mount IC change because radiative heat fix at board. It is reference data below, Evaluate IC in the set.

1. JEDEC51-7 standard

Board size114.3mm×76.2mm t=1.6mmCopper foil area 80%Power dissipation1250mWTa=25°C (It is reference value measured by JEDEC51-7 standard.)



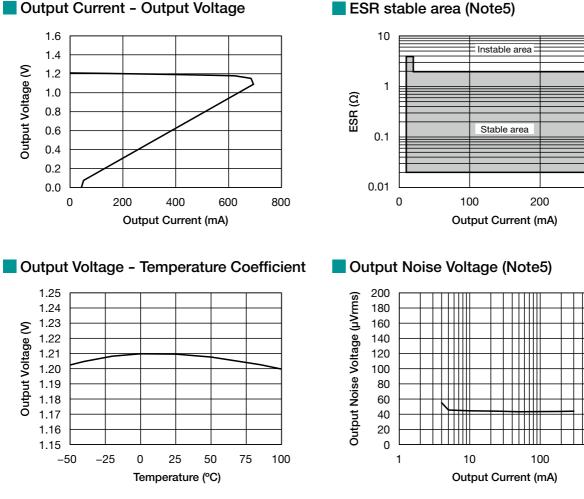
It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate).

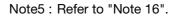
By increasing these copper foil pattern area of PCB, Power dissipation improves.

#### Characteristics (VOUT=1.2V) (Except where noted otherwise VDD=VOUT(TYP.)+1V, VCE=VDD, Ta=25°C) Input Voltage - Output Voltage Input Voltage - Input Current R∟=∞ 100 1.6 90 1.4 RL=1.2k 80 **Output Voltage (V)** Input Current (µA) 1.2 70 1.0 60 RL=8 0.8 50 40 0.6 RL=4 30 0.4 20 0.2 10 0.0 0 0 1 1 2 3 4 5 6 0 2 3 4 5 6 Input Voltage (V) Input Voltage (V) Load Regulation Line Regulation R∟=1.2kΩ 40 6 30 4 Load Regulation (mV) Line Regulation (mV) 20 2 10 0 0 -10 -2 -20 \_4 -30 -40 -6 3 0 100 200 300 0 1 2 4 5 6 **Output Current (mA)** Input Voltage (V) Ripple Rejection 0 -10 Ripple Rejection (dB) -20 Ш -30 -40 111 RL=8 -50 R∟=40 ### , TIN -60 -70 -80 0.1 10 100 1000 0.01 1 Frequency (kHz)

300

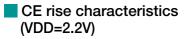
1000

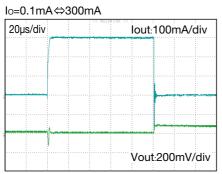




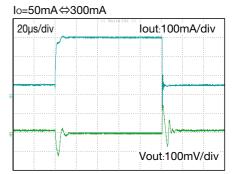
# Output Current - Output Voltage

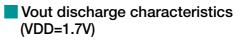
o= <b>50mA⇔300</b> m	ιA
20µs/div	lout:100mA/div
	Vout:50mV/div

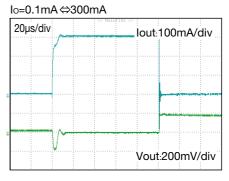




#### (VDD=1.7V)





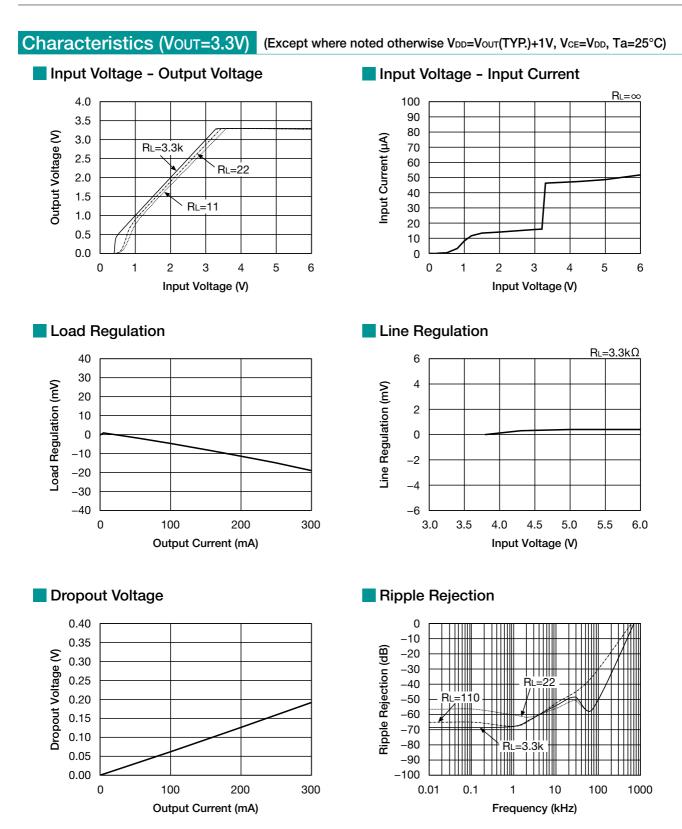


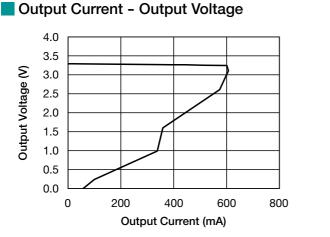
#### CE rise characteristics (VDD=2.2V, CE=0V→VDD, RL=120Ω)

20µs/div		<< MainFluk >>	
			CE:2V/div
	$\sim$	-	
			Vout:0.5V/div
	/		
			lin:500mA/div

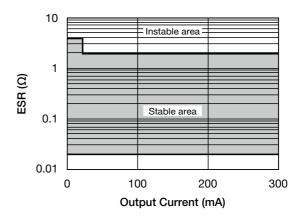
#### Vout discharge characteristics (VDD=2.2V, CE=VDD→0V)

20µs/div	<< Main#10k >	>
		CE:2V/div
		Vout:0.5V/div

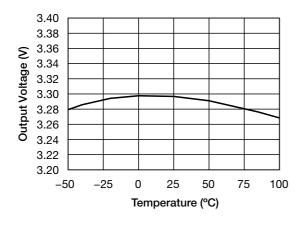




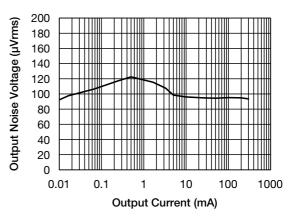
ESR stable area



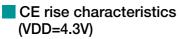
#### Output Voltage - Temperature Coefficient





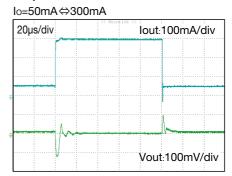


lo=50mA⇔300m	A
20µs/div	lout:100mA/div

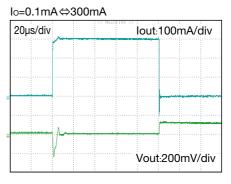


# Io=0.1mA⇔300mA

#### (VDD=3.8V)



# Vout discharge characteristics (VDD=3.8V)

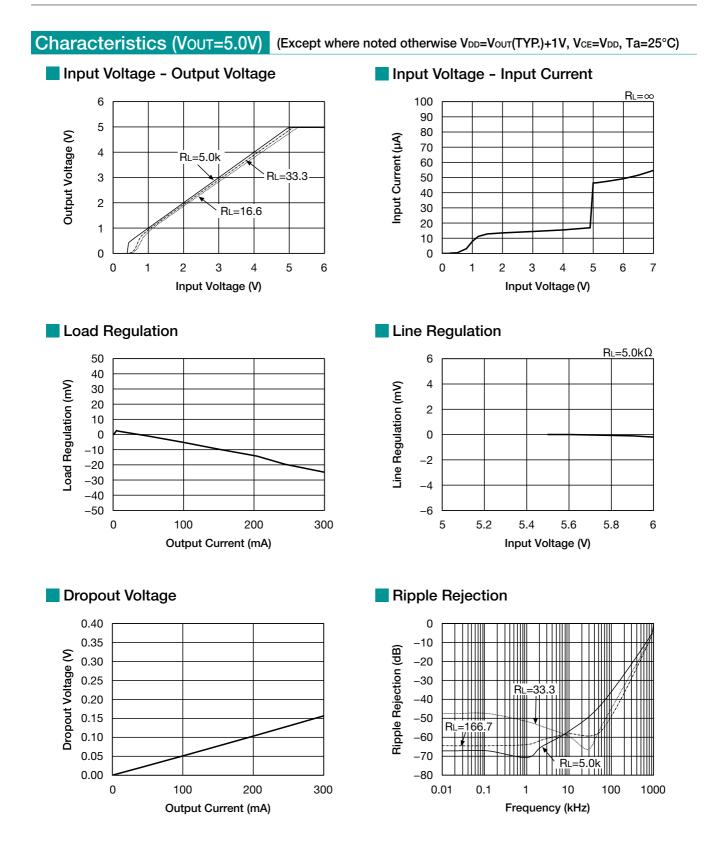


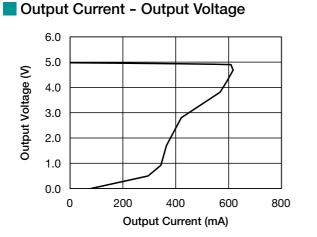
#### CE rise characteristics (VDD=4.3V, CE=0V→VDD, RL=300Ω)

20µs/div		<< Main310k >>
Ŧ		CE:5V/div
	$\int$	Vout:2V/div
-	X	lin:500mA/div
*		

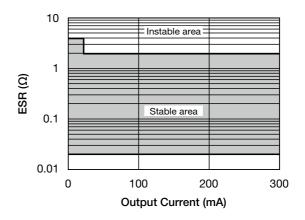
#### Vout discharge characteristics (VDD=4.3V, CE=VDD→0V)

20µs/div	Band 10k 35
	CE:5V/div
	Vout:2V/div

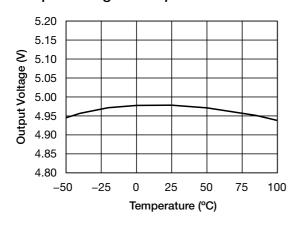




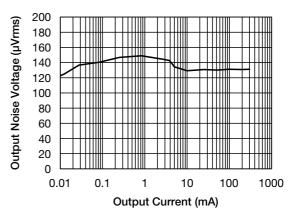
ESR stable area



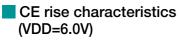
#### Output Voltage - Temperature Coefficient



#### Output Noise Voltage

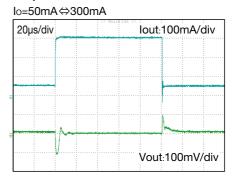


lo=50mA⇔300m	A
20µs/div	lout:100mA/div
	h

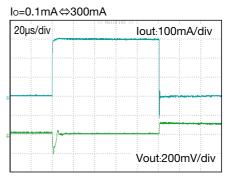


# Io=0.1mA⇔300mA

#### (VDD=5.5V)



# Vout discharge characteristics (VDD=5.5V)



#### CE rise characteristics (VDD=6.0V, CE=0V→VDD, RL=500Ω)

20µs/div		<< Mainilok :	2
T.			CE:5V/div
	1		Vout:2V/div
+			
	A		lin:500mA/div
÷			

#### Vout discharge characteristics (VDD=6.0V, CE=VDD→0V)

20µs/div	< Main210k >>
	CE:5V/div
	Vout:2V/div